Parameter Design of Voltage Balancing Circuit for Series Connected HV-IGBTs

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Abstract—**Applying power semiconductor devices in series connection is a direct and effective scheme to improve the voltage rating and power rating of power electronic converter. The key issue of device series connection is voltage balancing in static switching state and dynamic switching state. Active clamping circuit samples overvoltage on insulated gate bipolar transistor (IGBT), injects current into the gate and thus could increase the gate voltage and suppress the overvoltage effectively. In this paper, a voltage balancing circuit for high voltage IGBT (HV-IGBT) series connection is presented. The voltage balancing circuit is composed of static state voltage balancing sub-circuit across collector and emitter, dynamic state voltage balancing sub-circuit across collector and emitter and active clamping sub-circuit across collector and gate. The functions and principles of the three sub-circuits are then described. Besides the topology, the parameters of the voltage balancing circuit influence the voltage balance of series connected HV-IGBTs seriously. Based on quantitatively analyzing the relationships among the parameters of HV-IGBTs, the parameters of voltage balancing circuit and the voltage balancing indexes of the series connected devices, a parameter design method for the presented voltage balancing circuit is proposed. This parameter design method comprehensively considers the switching loss of HV-IGBT, the loss of voltage balancing circuit, the electrical stress on HV-IGBT and the switching frequency in order to guarantee the efficiency, reliability and performance of the system. The proposed parameter design method is applied to the development process of a series connection circuit with Infineon 6500V/600A HV-IGBTs. Experimental results verify the validity and feasibility of the proposed method.**

Keywords-HV-IGBT; series connection; voltage balancing; parameter design; active clamping

I. INTRODUCTION

In the recent years, as the rapid development of high power converters and their applications, the contradiction between the requirement of system voltage and the voltage rating of power semiconductor devices is more and more outstanding. There are mainly three kinds of measures to improve the rated voltage of power electronic converter under the current device voltage rating, which are employing transformers at the input and output of converter, adopting multilevel topology and applying devices in series connection. However, employing transformers would severely increase the volume and cost of converter, adopting multilevel topology with five or more voltage levels would complicate the structure and control of converter.

Applying power semiconductor devices in series connection is the equivalent of constructing a device which has higher voltage rating than the normal device. Theoretically, applying devices in series connection is the most direct, effective, and lowcost measure to increase the rated voltage of power electronic equipment [1].

Compared with other high power semiconductor devices such as gate turn-off thyristor (GTO) and integrated gate commutated thyristor (IGCT), insulated gate bipolar transistor (IGBT) shows its superiorities in switching speed, switching loss, driving complicacy, etc. Therefore, IGBTs are widely used in high power converters. Recently, voltage rating of IGBT increases continuously. In this paper, high voltage IGBT (HV-IGBT) refers to IGBT with the maximum collector-emitter voltage (V_{CES}) equal to or higher than 3300V. Even though Infineon Technologies and Mitsubishi Electric both have produced HV-IGBTs with $V_{CES} = 6500$V, two level converters using HV-IGBTs still cannot be directly connected to 6kV power system without transformer or series connection of devices.

In order to guarantee the safe operation of series connected power semiconductor devices and the reliability of converter, voltage balancing circuit must be introduced. The function of voltage balancing circuit is distributing dc-bus voltage of the converter as equally as possible to every series connected device and avoiding overvoltage of any device in both static switching state and dynamic switching state. Generally, the voltage balancing circuits for series connected IGBTs now available can be classified into two categories, which are collector-emitter side and gate side [2-3]. Collector-emitter side voltage balancing circuit, which is connected across the collector and emitter of each IGBT, includes three types, passive snubber circuit [4-6], resonance snubber circuit [7], and clamping circuit [8-10]. From the standpoint of energy, collector-emitter side circuit absorbs a part of the unbalanced energy that is corresponding to the unbalanced voltage and dissipates it outside of IGBT. Therefore the switching loss of IGBT doesn't increase. However, the loss of collector-emitter side circuit cannot be ignored. Gate side voltage balancing circuit, including active control circuit [11-13], synchronous control circuit [14-15], and active clamping circuit [16-20], makes the unbalanced energy consumed in IGBT by adjusting the gate voltage, gate current or switching time of series connected IGBTs. The loss of gate side circuit is low. However,

in order to suppress the collector-emitter voltage, gate side circuit controls the IGBT to briefly operate in active region. Therefore the switching loss and switching time of the IGBT would increase.

In this paper, according to the features of HV-IGBT, a voltage balancing circuit for HV-IGBT series connection, which combines collector-emitter side circuit and gate side circuit, is presented. A parameter design method for this voltage balancing circuit is then proposed based on theoretically deriving the performance indexes from the parameters of HV-IGBT and the circuit. Experimental waveforms show that the proposed method ensures the remarkable voltage balancing effect of the presented circuit.

II. VOLTAGE BALANCING CIRCUIT FOR SERIES CONNECTED HV-IGBTS

Compared with normal IGBT whose V_{CES} is equal to or lower than 1700V, the switching loss of HV-IGBT is much higher. Therefore the unbalanced energy, corresponding to the unbalanced voltage in HV-IGBT series connection, is higher and more concentrated.

When applied to HV-IGBT series connection alone for voltage balancing, the collector-emitter side circuit needs to absorb and dissipate the high unbalanced energy and thus its loss might be unbearably high. Moreover, because collector-emitter side circuit is in parallel with HV-IGBT, the components of this kind of voltage balancing circuit, such as non inductive capacitor and fast recovery diode, must withstand the same high voltage as HV-IGBT does. Hence the selection of the components of collector-emitter side circuit is extremely difficult.

If series connected HV-IGBTs adopt gate side circuit alone for voltage balancing, because of the high switching loss and long switching time caused by the transient operation in active region, the efficiency and switching frequency of the converter are limited, which would lead to deterioration of the system performances.

Based on the consideration mentioned above, a voltage balancing scheme for HV-IGBT series connection is designed as shown in Fig. 1. It can be seen that this voltage balancing scheme is the combination of collector-emitter side circuit and gate side circuit. At the collector-emitter side, considering the difficulty in the selection of components, a resistor and a RC snubber are adopted as the static state voltage balancing sub-circuit and the dynamic state voltage balancing sub-circuit, respectively. At the gate side, in order to avoid using components with high isolation voltage and complicated driver circuit, which are necessary for active control circuit and synchronous control circuit, active clamping circuit is employed. Based on the proper circuit parameters, this voltage balancing scheme could reasonably distribute the unbalanced energy corresponding to the unbalanced voltage of series connected HV-IGBTs and thus could limit the losses of HV-IGBT and its external circuit under the acceptable level. Furthermore, with the aid of collector-emitter side circuit, the negative effect of gate side circuit on the switching time of HV-IGBT is weakened. Hence the switching frequency could be improved.
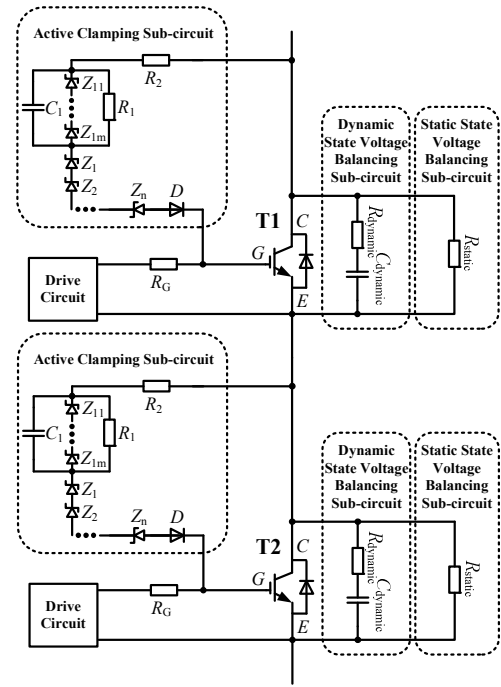

Figure 1. Voltage balancing scheme for HV-IGBT series connection.

III. PARAMETER DESIGN METHOD

A. Static State Voltage Balancing Sub-circuit

In the off state of series connected HV-IGBTs, the voltage unbalance is mainly caused by the variance of collector-emitter cut-off currents (I_{CES}) of HV-IGBTs. In other words, difference between off state equivalent resistances, which can be defined as $R_{off} = V_{CES}/I_{CES}$, leads to the off state voltage unbalance. Therefore, the general method for static state voltage balancing is connecting a resistor, whose resistance is much lower than R_{off}, in parallel with each HV-IGBT. This resistor is named static state voltage balancing resistor R_{static}. HV-IGBT with higher I_{CES} has lower R_{off}. In order to achieve better static state voltage balancing effect, the highest I_{CES} should be applied to the calculation of R_{static}.

In the condition of two HV-IGBTs (T1 and T2) series connection, assuming

$$I_{CES1} < I_{CES2}, \qquad (1)$$

that is,

$$R_{off1} > R_{off2}. \qquad (2)$$

T1 withstands higher off state voltage than T2. In order to ensure that the off state voltage unbalance ratio is less than 10%, it is required that

$$\frac{R_{static} \cdot V_{CES}/I_{CES1}}{R_{static} + V_{CES}/I_{CES1}} < \frac{R_{static} \cdot V_{CES}/I_{CES2}}{R_{static} + V_{CES}/I_{CES2}} \cdot 110\% . \qquad (3)$$

Moreover, the voltage on T1 mustn't exceed V_{CES}, that is,

$$V_{dc} \cdot \frac{\dfrac{R_{static} \cdot V_{CES}/I_{CES1}}{R_{static} + V_{CES}/I_{CES1}}}{\dfrac{R_{static} \cdot V_{CES}/I_{CES1}}{R_{static} + V_{CES}/I_{CES1}} + \dfrac{R_{static} \cdot V_{CES}/I_{CES2}}{R_{static} + V_{CES}/I_{CES2}}} < V_{CES}, \quad (4)$$

where V_{dc} represents dc-link voltage. Take the most adverse situation into account, namely $I_{CES1} = 0$, $I_{CES2} = I_{CESmax}$, where I_{CESmax} is the maximum value of I_{CES}, in order to satisfy (3) and (4), it is required that

$$R_{static} < \frac{0.1 V_{CES}}{I_{CESmax}}, \quad (5)$$

$$R_{static} < \frac{V_{CES}(2V_{CES} - V_{dc})}{I_{CESmax}(V_{dc} - V_{CES})}. \quad (6)$$

The resistance value of R_{static} can be determined through (5) and (6), while its rated power should satisfy

$$P_{Rstatic} > \frac{V_{dc}^2}{4R_{static}}. \quad (7)$$

B. Dynamic State Voltage Balancing Sub-circuit

In HV-IGBT series connection circuit, many factors might influence on the voltage balance during transient switching process. Therefore it is more difficult to implement voltage balancing in dynamic state. The simplest dynamic state voltage balancing circuit is connecting a capacitor $C_{dynamic}$ in parallel with each HV-IGBT. $C_{dynamic}$ limits the variation rate of collector-emitter voltage V_{CE} and thus could suppress the voltage unbalance in dynamic state. However, $C_{dynamic}$ would increase the peak current and loss of HV-IGBT in its switching on process. In order to solve this problem, a resistor $R_{dynamic}$ is brought in and connected in series with $C_{dynamic}$. But $R_{dynamic}$ would weaken the effect of voltage balancing in dynamic state and would introduce loss to the voltage balancing circuit. Connecting a fast recovery diode in parallel with $R_{dynamic}$ could avoid these drawbacks of RC snubber circuit to some extent. However, the fast recovery diode must have the same voltage rating as HV-IGBT. The lectotype of the required diode is extremely difficult. Therefore, the RC snubber, which is composed of $C_{dynamic}$ and $R_{dynamic}$, is adopted as the dynamic state voltage balancing sub-circuit for HV-IGBT series connection as shown in Fig. 1. There are two ways to design the parameter of $C_{dynamic}$. One way is considering the mismatch of HV-IGBT characteristics while the other way focused on the asynchronism of drive circuits.

From the view of device characteristics, the dynamic state voltage unbalance is caused by the mismatch of reverse recovered charge Q_{rr} of the antiparallel diodes in the series connected HV-IGBT modules. Assuming

$$Q_{rr1} < Q_{rr2}, \quad (8)$$

during the switching off process, the load current charges the junction capacitor of HV-IGBT and $C_{dynamic}$, the unbalanced voltage can be expressed as

$$\Delta V = \frac{\Delta Q}{C_{dynamic}} = \frac{Q_{rr2} - Q_{rr1}}{C_{dynamic}}. \quad (9)$$

In the dynamic state, it must be guaranteed that the voltage on T1 is lower than V_{CES}, that is

$$\frac{V_{dc} + \Delta V}{2} < V_{CES}. \quad (10)$$

Considering the most adverse situation which is $Q_{rr1} = 0$ while $Q_{rr2} = Q_{rrmax}$, where Q_{rrmax} is the maximum value of Q_{rr}, combining (9) and (10), it is obtained that

$$C_{dynamic} > \frac{Q_{rrmax}}{2V_{CES} - V_{dc}}. \quad (11)$$

From the view of drive asynchronism, the dynamic state voltage unbalance is caused by the delay between switching times of the series connected HV-IGBTs. Assuming the maximum delay time is Δt_{max} and the current of HV-IGBT is I_C, then the maximum unbalanced voltage during the dynamic process is deduced as

$$\Delta V = \frac{\Delta t_{max} \cdot I_C}{C_{dynamic}}. \quad (12)$$

In order to guarantee the voltages on HV-IGBTs are lower than V_{CES}, it is required that

$$C_{dynamic} > \frac{\Delta t_{max} \cdot I_C}{2V_{CES} - V_{dc}}. \quad (13)$$

During the on state of HV-IGBT, $C_{dynamic}$ should be totally discharged through $R_{dynamic}$, therefore it should be satisfied that

$$R_{dynamic} < \frac{T_{ONmin}}{3C_{dynamic}}, \quad (14)$$

where T_{ONmin} is minimum pulse width of HV-IGBT. The rated power of $R_{dynamic}$ is required as

$$P_{Rdynamic} > \frac{C_{dynamic} V_{CES}^2}{2} \cdot f_s, \quad (15)$$

where f_s refers to the switching frequency of HV-IGBT.

In HV-IGBT series connection circuit, because of the high power density, $P_{Rdynamic}$ calculated through (11), (13) and (15) is usually several kilowatts, which would seriously reduce the efficiency of the system and thus is unacceptable. In this case, the parameter design flow should be reversed, that is, determine a proper $P_{Rdynamic}$ first, then calculate $C_{dynamic}$ by (15), lastly using (14) to obtain $R_{dynamic}$. In this way, the calculated $C_{dynamic}$ may not satisfy (11) or (13), the insufficient of dynamic state voltage balancing effect would be compensated by the active clamping sub-circuit at the gate side of HV-IGBT.

C. Active Clamping Sub-circuit

As mentioned above, because of the limit of loss, the collector-emitter side circuits usually cannot provide sufficient voltage balancing effect to series connected HV-IGBTs in dynamic state. Furthermore, under some special condition such as overcurrent and dc-link overvoltage, the collector-emitter side circuits cannot ensure that voltages on HV-IGBTs are all lower than V_{CES}. Therefore, gate side voltage balancing circuits are indispensable to HV-IGBT series connection.

The gate side circuit shown in Fig. 1 is a combination and improvement of the basic Zener diode active clamping scheme and the scheme of increasing Miller capacitor. Defining the total breakdown voltage of the series connected Zener diodes Z_1 to Z_n is V_{Z1}, the total breakdown voltage of Z_{11} to Z_{1m} is V_{Z2}, considering the collector-emitter voltage V_{CE} is approximately equal to the collector-gate voltage of HV-IGBT, the switching off process of HV-IGBT with the active clamping sub-circuit can be divided into three phases, as shown in Fig. 2.

In phase1, V_{CE} is lower than V_{Z1}, the active clamping sub-circuit doesn't effect on the HV-IGBT, V_{CE} increases rapidly.

In phase2, V_{CE} is higher than V_{Z1}, Zener diodes Z_1 to Z_n are broken down, the collector of HV-IGBT charges C_1 through R_2, Z_1 to Z_n, and D, therefore the rising rate of V_{CE} is reduced and the voltage unbalance is restrained dynamically. In this phase, the effect of active clamping sub-circuit is equivalent to a capacitor which is connected across the collector-gate enhancing the Miller effect of HV-IGBT.
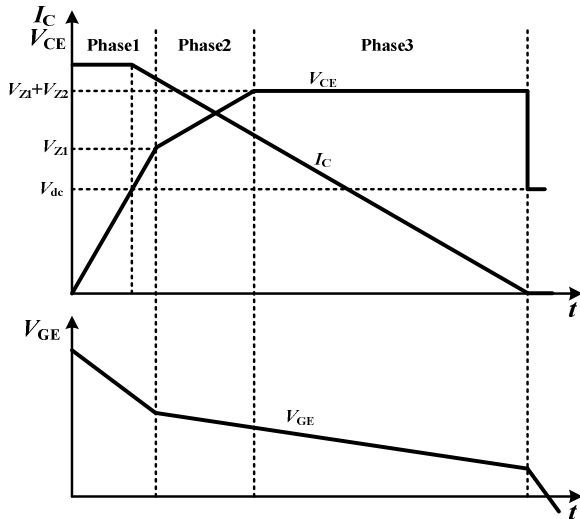

Figure 2.   Switching off process with active clamping sub-circuit.

In phase3, V_{CE} reaches $V_{Z1}+V_{Z2}$, Zener diodes Z_1 to Z_n and Z_{11} to Z_{1m} are all broken down. Considering the voltage drop on R_2, V_{CE} is clamped at the voltage which is a little higher than $V_{Z1}+V_{Z2}$ until the energy stored in stray inductance of the commutation circuit is totally consumed, and then the switching off process is finished.

During phase2 and phase3, the active clamping sub-circuit injects current into the gate of HV-IGBT and makes it operate in active region, thus the voltage spike of V_{CE} is suppressed. However, the loss of HV-IGBT increases rapidly and the switching speed is slowed down in these two phases. Consequently, two requirements should be satisfied simultaneously through the parameter design of active clamping sub-circuit. First, the sub-circuit must limit the voltage on HV-IGBT lower than its V_{CES} and restrain the overvoltage of device. Second, frequent actions of the active clamping sub-circuit must be avoided in order to reduce the loss and the switching time of HV-IGBT.

In the condition of two HV-IGBTs series connection, according to the analyses above, the two threshold values (V_{Z1} and $V_{Z1}+V_{Z2}$) of active clamping sub-circuit are designed as

$$0.6V_{dc} < V_{Z1} < 0.65V_{dc}, \tag{16}$$

$$0.65V_{dc} < V_{Z1} + V_{Z2} < 0.75V_{dc}. \tag{17}$$

Meanwhile, in order to avoid the overvoltage of HV-IGBT,

$$V_{Z1} + V_{Z2} < V_{CES}. \tag{18}$$

Furthermore, in order to suppress the frequent actions of active clamping, V_{Z1} is required to be higher than the peak voltage of the normal switching off process, that is,

$$V_{Z1} > \frac{1}{2}(V_{dc} + 0.8L_s I_C / t_f). \tag{19}$$

where L_s refers to the stray inductance of commutating loop and t_f represents the fall time of HV-IGBT.

The function of resistor R_2 is limiting the current in the active clamping sub-circuit, thus it is required that

$$R_2 > \frac{V_{dc} - V_{Z1}}{I_Z}, \tag{20}$$

where I_Z is the maximum current of the Zener diodes.

After confirming R_2 and the parameters of dynamic state voltage balancing sub-circuit, the rising rate of V_{CE} in phase2 mainly depends on the parameter C_1. The larger C_1 is, more slowly V_{CE} rises, and the longer the duration of phase2 is. Parameter C_1 should be designed through the simulation considering the characteristics of HV-IGBT.

After the end of switching off process, C_1 is discharged through the resistor R_1. This discharging must finish before the next switching off process, thus the parameter R_1 should satisfy

$$R_1 < \frac{T_s}{3C_1} = \frac{1}{3C_1 f_s} . \qquad (21)$$

It can be concluded from the design procedure above that under the normal condition, the active clamping sub-circuit would not enter phase2 and phase3 during switching off processes, voltage balancing of series connected HV-IGBTs is implemented by the collector-emitter side circuits. Therefore, normally the active clamping sub-circuit does not effect on V_{CE}, which ensures the switching speed and avoids high switching losses of HV-IGBTs. Under special conditions when collector-emitter side circuits cannot reliably suppress high V_{CE} or high dV_{CE}/dt, the active clamping sub-circuit turns into phase2 and phase3, and limits V_{CE} to the voltage lower than V_{CES}.

IV. EXPERIMENTAL RESULTS

The proposed parameter design method is applied to the development process of a HV-IGBT series connection test platform which is shown in Fig. 3(a) with 6500V/600A HV-IGBTs (Infineon FZ600R65KF1). Fig. 3(b) presents a module of the test platform including one HV-IGBT, its drive circuit, heat sink, static state voltage balancing sub-circuit, dynamic state voltage balancing sub-circuit and active clamping sub-circuit.

Fig. 4, Fig. 5, Fig. 6, Fig. 7 and Fig. 8 are experimental waveforms of the HV-IGBT series connection test platform. In these experiments, V_{dc} = 400V, I_C = 50A, V_{CE1} and V_{CE2} refer to collector-emitter voltages of T1 and T2 respectively, V_{GE1} represents gate voltage of T1, I_{clamp} is the current of active clamping circuit of T1, two threshold values of the active clamping sub-circuits are V_{Z1} = 280V and $V_{Z1}+V_{Z2}$ = 313V. Due to the limit of oscilloscope channel number, the waveforms of gate voltage and active clamping circuit current of T2 are not presented in these figures.

Fig. 4 shows the switching off waveforms when T1 and T2 have the same switching signal (no delay). It can be seen that because of the inherent differences between the characteristics of series connected HV-IGBTs and their drive circuits, the waveforms of V_{CE1} and V_{CE2} during the switching off process are slightly different. V_{CE2} is higher than V_{CE1} but does not reach the threshold value V_{Z1}. Hence the active clamping sub-circuits operates in phase1 only, there are low current ripples in the waveform of I_{clamp} which are caused by the charging and discharging of the equivalent capacitors of Zener diodes in the active clamping sub-circuits.

Fig. 5 and Fig. 7 present the switching off waveforms without active clamping sub-circuits when the switching signal of T2 is delayed for 1μs and 2μs compared with that of T1, respectively. T1 switches off earlier than T2 and thus withstands extremely high voltage V_{CE1}.

Fig. 6 and Fig. 8 show the switching off waveforms with active clamping sub-circuits when the switching signal of T2 is delayed for 1μs and 2μs, respectively. Because V_{CE1} exceeds the two threshold values, the active clamping sub-circuit of T1 enters phase2 and phase3 during the switching off process, the sub-circuit injects current into the gate of T1 and increases V_{GE1}, thus V_{CE1} is clamped at the voltage which is a little higher than $V_{Z1}+V_{Z2}$.

Comparing Fig. 5 with Fig. 6 and Fig. 7 with Fig. 8, the active clamping sub-circuit suppresses the voltage spike, reduces the voltage unbalance ratio of the series connected HV-IGBTs and hence improves the reliability of the system effectively.
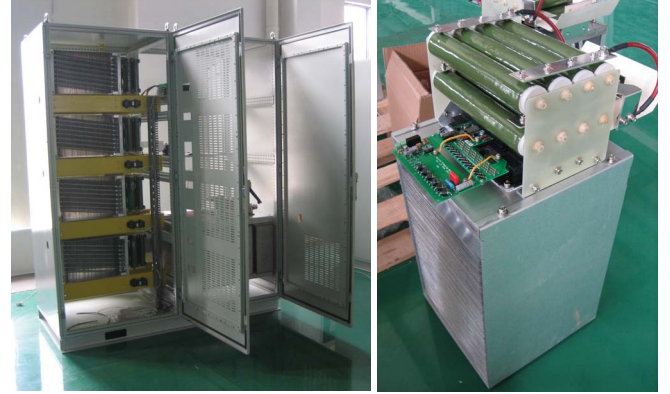
(a) Cabinet   (b) Module

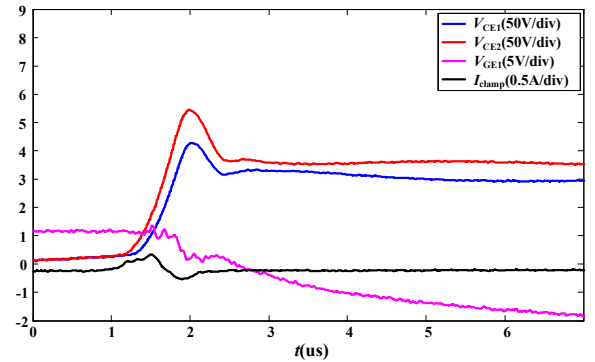Figure 3. HV-IGBT series connection test platform.

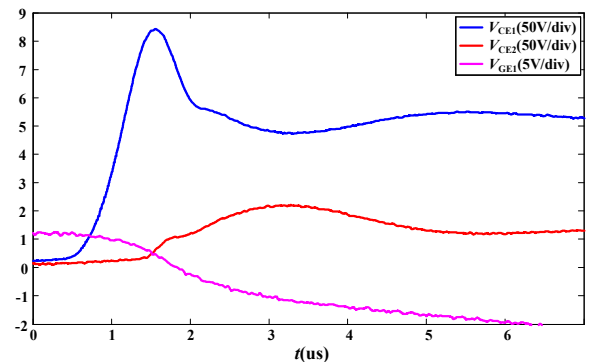Figure 4. Switching off waveforms with active clamping sub-circuit (no delay).

Figure 5. Switching off waveforms without active clamping sub-circuit (1μs delay).
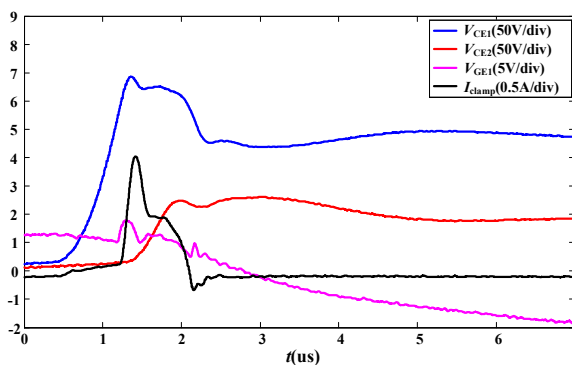
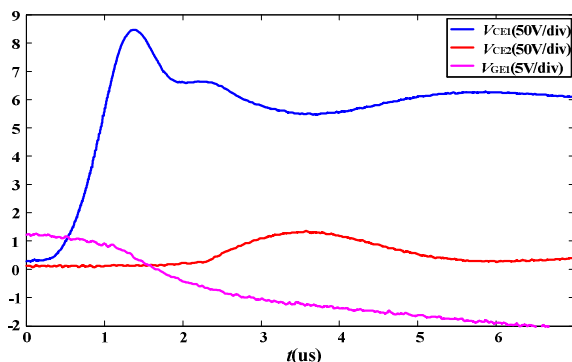Figure 6. Switching off waveforms with active clamping sub-circuit
(1μs delay).

Figure 7. Switching off waveforms without active clamping sub-circuit
(2μs delay).

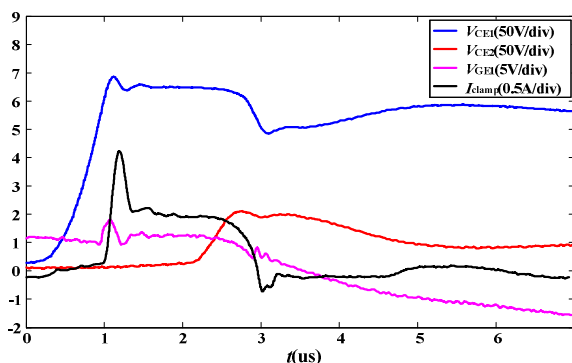Figure 8. Switching off waveforms with active clamping sub-circuit
(2μs delay).

V. CONCLUSION

This paper presented a voltage balancing circuit for series connected HV-IGBTs, described its component parts and analyzed the operation principle of each sub-circuit. Based on the quantificational deductions, the parameter design method for the voltage balancing circuit was proposed considering the efficiency, reliability and performance of the system. The proposed parameter design method was implemented and verified in an actual HV-IGBT series connection test platform. Experimental results proved that the proposed method was valid and feasible for HV-IGBT series connection.

REFERENCES

[1] Y. Shakweh and E. A. Lewis, "Assessment of medium voltage PWM VSI topologies for multi-megawatt variable speed drive applications," 30th Annual Power Electronics Specialist Conf., vol. 2, pp. 965–971, July 1999.

[2] P. R. Palmer and A. N. Githiari, "The series connection of IGBT's with active voltage sharing," IEEE Transactions on Power Electronics, vol. 12, no. 4, pp. 637-644,1997.

[3] N. Y. A. Shammas, R. Withanage and D. Chamund, "Review of series and parallel connection of IGBTs," IEE Proc. Circuits Devices Syst., vol. 153, no. 1, pp. 34-39, 2006.

[4] J. F. Chen, J. N. Lin and T. H. Ai, "The techniques of the serial and paralleled IGBTs," IEEE IECON'96, pp. 999-1004, 1996.

[5] T. Nakajima, H. Suzuki, Y. Tamura, et al., "Development of IEGT series and parallel connection technology for high power converters," IPEC'00, pp. 670-675, 2000.

[6] K. Sung, H. Akiyama, K. Takao, et al., "Switching characteristic of Si-IEGT and SiC-PiN diode pair connected in series," IPEC'10, pp. 170-175, 2010.

[7] D. M. Divan and G. Skibinski, "Zero-switching-loss inverters for high-power applications," IEEE Transactions on Industry Applications, vol. 25, no. 4, pp. 634-643, 1989.

[8] B. Bijlenga, "Protective circuit for series-connected power semiconductors," United States Patent, 5946178, 1999.

[9] G. Busatto, B. Cascone, L. Fratelli, et al., "Series connection of IGBTs in hard-switching applications," Industry Applications Conf., vol. 2, pp. 825-830, 1998.

[10] F. V. Robinson and V. Hamidi, "Series connecting devices for high-voltage power conversion," UPEC'07, pp. 1205-1210, 2007.

[11] A. Raciti, G. Belverde, A. Galluzzo, et al., "Control of the switching transients of IGBT series strings by high-performance drive units," IEEE Transactions on Industry Electronics, vol. 48, no. 3, pp. 482-490, 2001.

[12] P. R. Palmer and A. N. Githiari, "The series connection of IGBT's with optimized voltage sharing in the switching transisent," PESC'95, pp. 44-50, 1995.

[13] S. Hong, V. Chitta, and D. A. Torrey, "Series connection of IGBT's with active voltage balancing," IEEE Transactions on Industry Applications, vol. 35, no. 4, pp. 917-923, 1999.

[14] K. Sasagawa, Y. Abe, and K. Matsuse, "Voltage balancing method for IGBTs connected in series," Industry Applications Conf., vol. 4, pp. 2597-2602, 2002.

[15] C. Gerster, "Fast high-power/high-voltage switch using series-connected IGBTs with active gate-controlled voltage-balancing," APEC'94, vol. 1, pp. 469-472, 1994.

[16] M. Bruckmann, R. Sommer, M. Fasching, et al., "Series connection of high voltage IGBT modules," Industry Applications Conf., vol. 2, pp. 1067-1072, 1998.

[17] H. Rüedi and P. köhli, "SCALE driver for high voltage IGBTs," PCIM'99, pp. 357-364, 1999.

[18] J. Saiz, M. Mermet. D. Frey, et al., "Optimisation and integration of an active clamping circuit for IGBT series association," Industry Applications Conf., vol. 2, pp. 1046-1051, 2001.

[19] A. Piazzesi and L. Metsenc, "Series connection of 3.3kV IGBTs with active voltage balancing," PESC'04, vol. 2, pp. 893-898, 2004.

[20] J. W. Baek, D. W. Yoo, and H. G. Kim, "High voltage switch using series-connected IGBTs with simple auxiliary circuit," IEEE Transactions on Industry Applications, vol. 37, no. 6, pp. 1832-1839, 2001.