

Replacement Transmitter System for USCG Loran Recapitalization

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Requirements and Understanding

- USCG issues Performance Specification
 - Meet and exceed COMDTINST M16562
 - Controlling factors
 - Remote operability
 - Future requirements
 - Reduced operational cost
- Megapulse understands this to mean
 - TTX not supportable in the near term (NSITNT)
 - SSX control circuits NSITLT
 - TTX/SSX don't support additional capabilities
 - Less bodies = Less \$

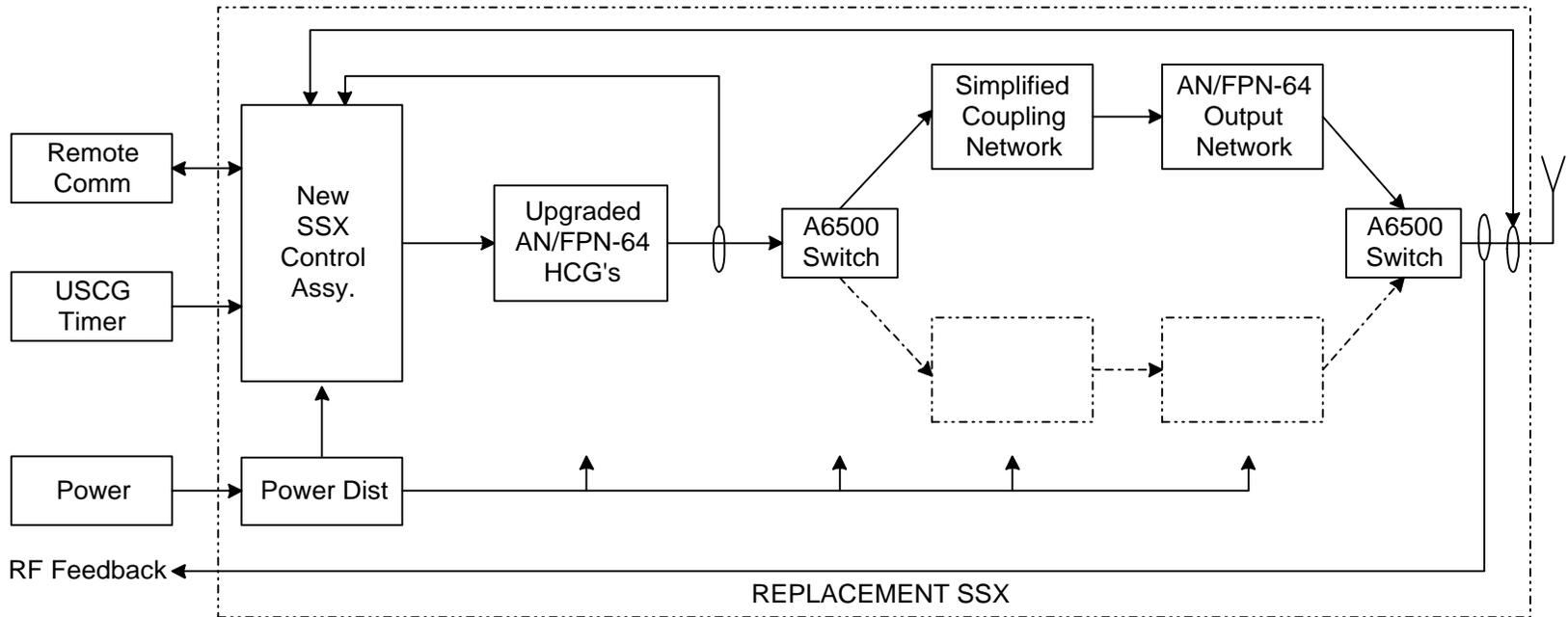


General Design Strategy

- Goal:
 - The Megapulse technical response shall describe a replacement transmitter based on the following design goals:
 - Further increase individual HCG output power through improved components
 - Modernize Control Console assembly
 - Make the number of DHC's variable and assignments flexible
 - Future incorporation of IFM should have minimal impact on proposed architecture
 - Maximize commonality with exiting USCG assemblies



General Design Block Diagram



MP3611-A.VSD



Modernizations AN/FPN-64, A6500

- Increased Output Power/Higher Efficiency
 - Demonstrated in A6500
 - Modern components available with higher ratings open possibility further



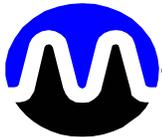
Modernization AN/FPN-64, A6500

- Increasing Flexibility of DHCs
 - Original SSX prototype used 10 DHCs
 - Timing & amplitude was controlled by a PDP-11
- Idea was Revisited During “Dual Pulse” Tests
 - A 52 μ sec time to peak Chayka pulse was generated using 4 DHCs
 - A 65 μ sec TTP Loran pulse was generated with 6 DHCs
 - Results published at Bonn DGON conf. Mar 2000
- DHCs that are Flexible and Reassigneable
 - ECD control will be more robust
 - Enhanced fail soft of HCG's
 - Allows for control of TTP



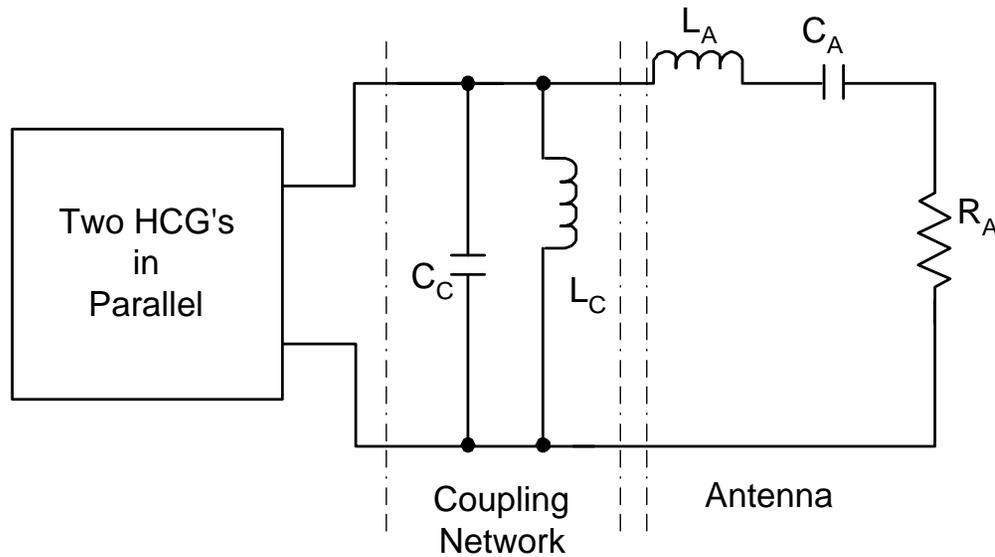
Design Verification Simulations & Tests

- Tests and Simulations were Performed to Verify Proposed Modernizations
 - Identify impact of increased voltages and currents (due to doubling the output power) on HCG components;
 - Ensure that Loran signal parameters (e.g. ECD, Tail Attenuation, etc) can be met with reduced number of HCG's.



High Power Test

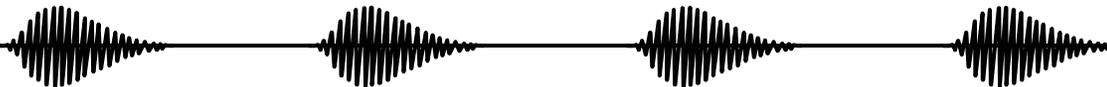
- Schematic of Experimental Test Setup



MP3600-1.VSD



Experimental Test Setup

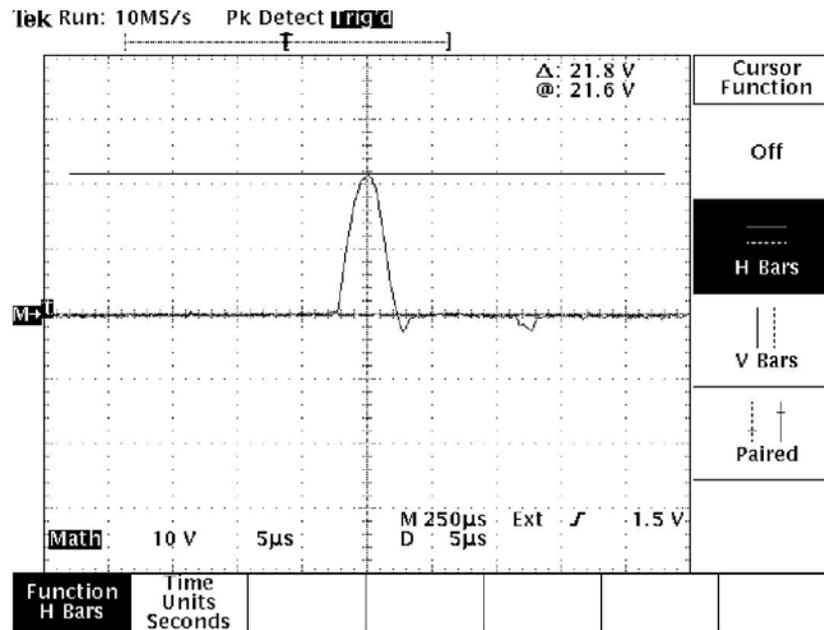


Experimental Test Setup (cont.)

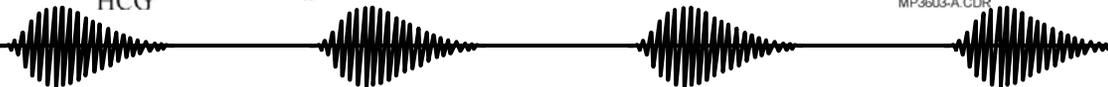


Design Verification Simulation & Tests

- HCG Current into Coupling Network



$$I_{HCG} = 872 \text{ Amps}$$

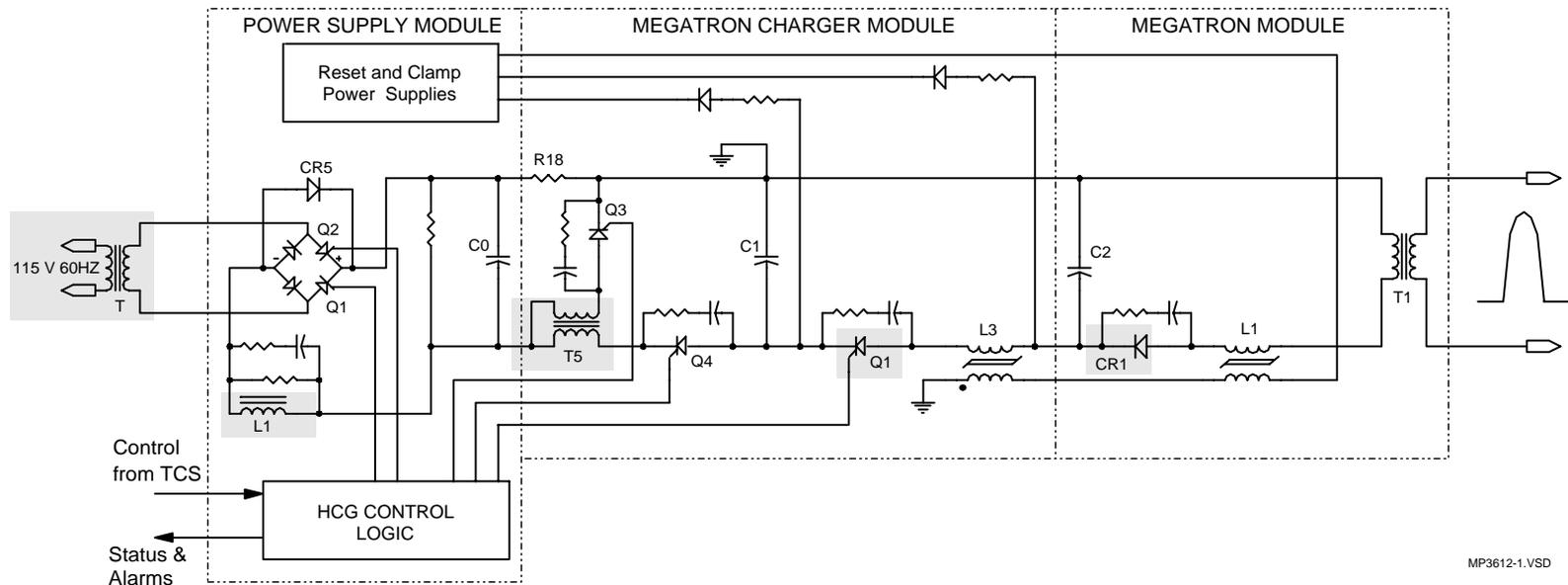


MP3603-A.CDR

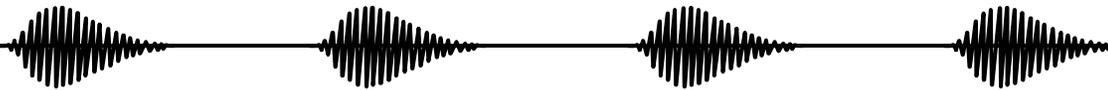


Design Verification Simulation & Tests

- Implications to Design of HCG
(identified by shaded areas below)



MP3612-1.VSD



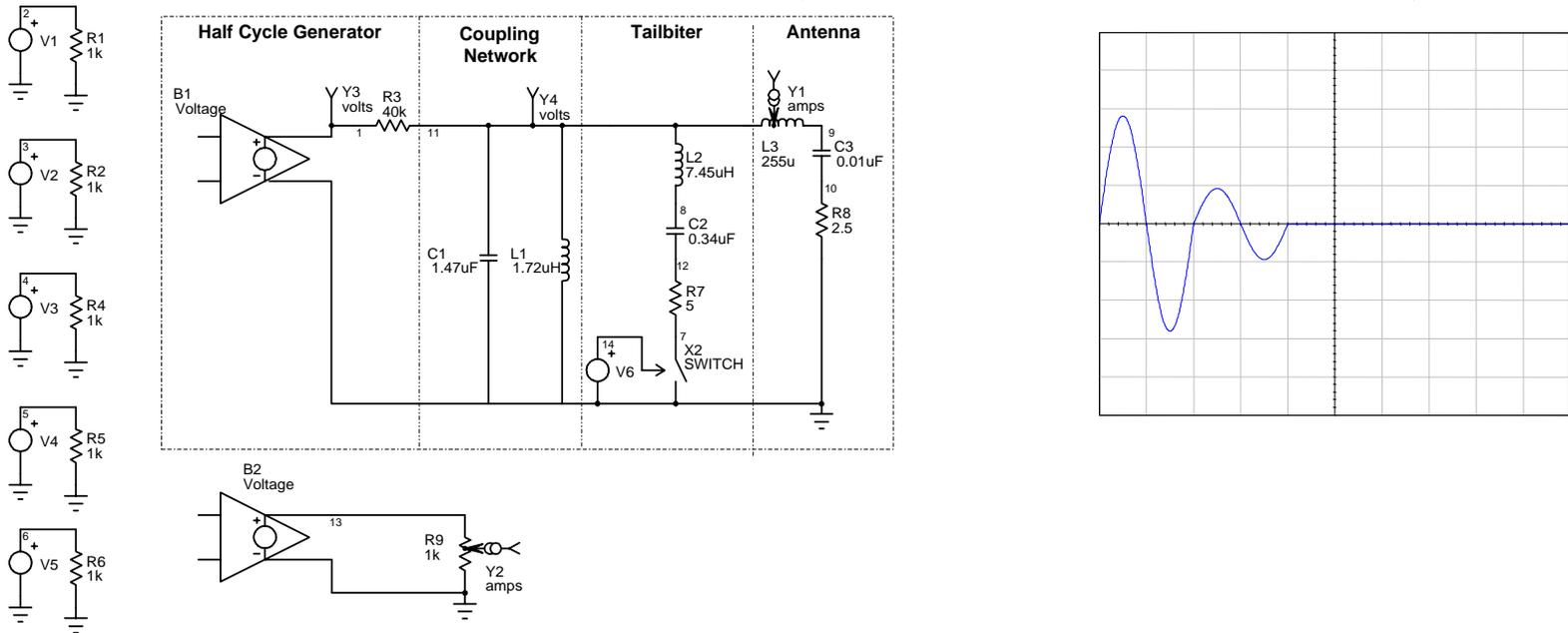
Design Verification Simulation & Tests

- IsSpice4 Software was used for Simulations
- 16 HCG Transmitter with 625ft TLM Antenna was Modeled
- Actual Cape Race Transmitter (32 HCG) Test Data was used as Reference to Validate Simulation Results
- Simulations Included:
 - Generations of Loran signals with full range of ECD's;
 - Verification of signal's tail attenuation (0.014A @ $t > 500\text{sec}$);
 - Signal's spectrum compliance to specification



Design Verification Simulation & Tests

- Simulation Schematic (16 HCG-625ft TLM)

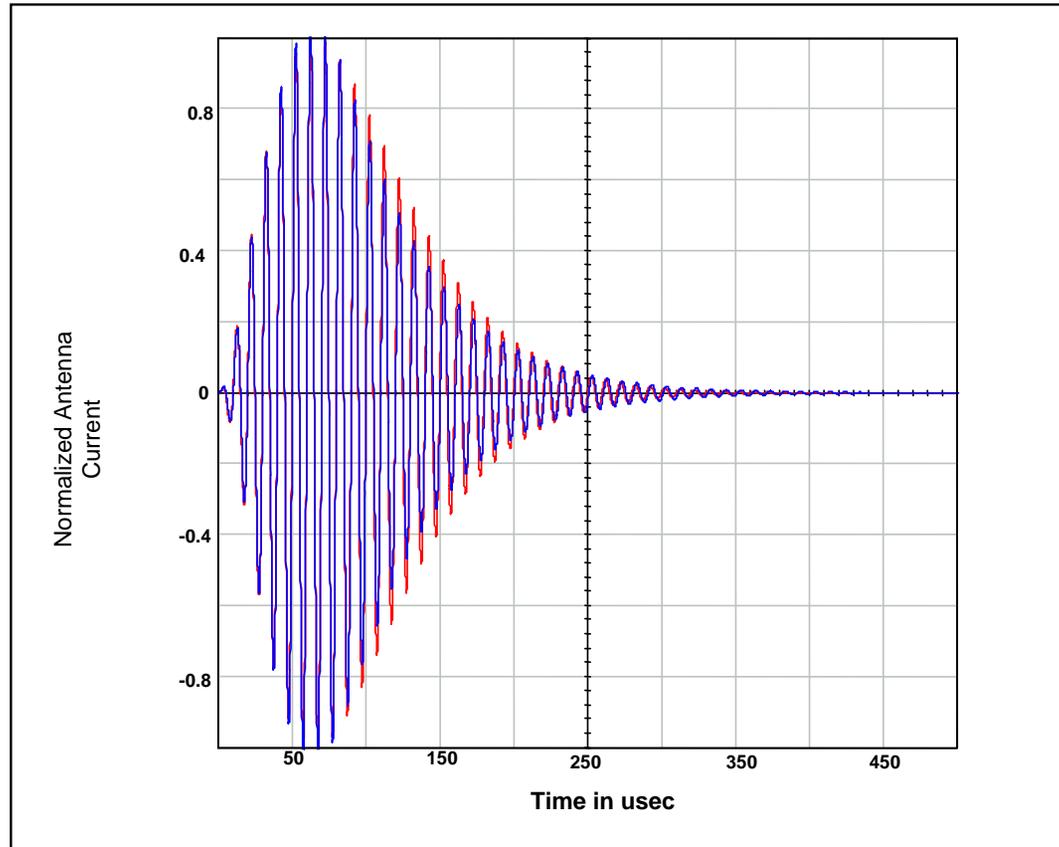


- **V1 – 100kHz Sinewave Generator**
- **V2 – V5 – Generate 5μsec wide pulses at 5μsec intervals**
- **B1 – DHC Generator = $V1*V2+V1*V3+V1*V4+V1*V5$;**
- **B2 – Loran-C Signal Generator (per COMDTINST M16562.4A specification)**



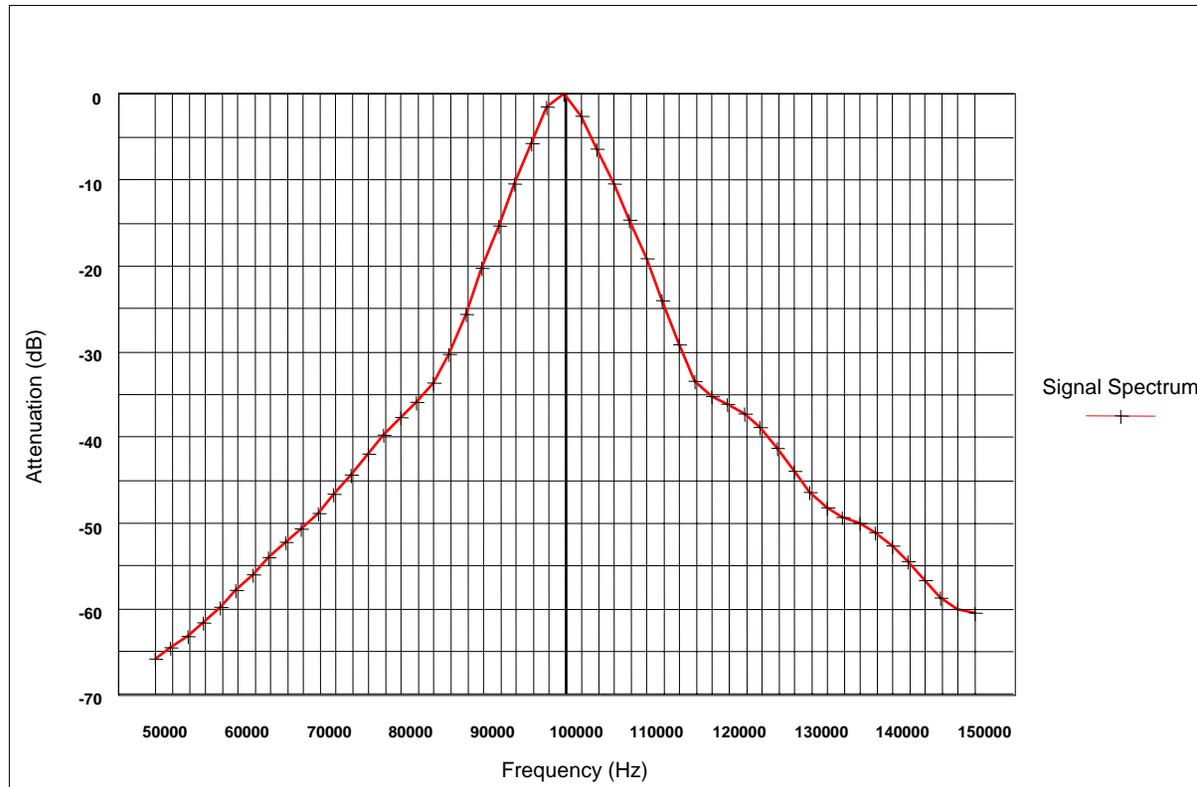
Design Verification Simulation & Tests

- Simulation Generated Loran Signal

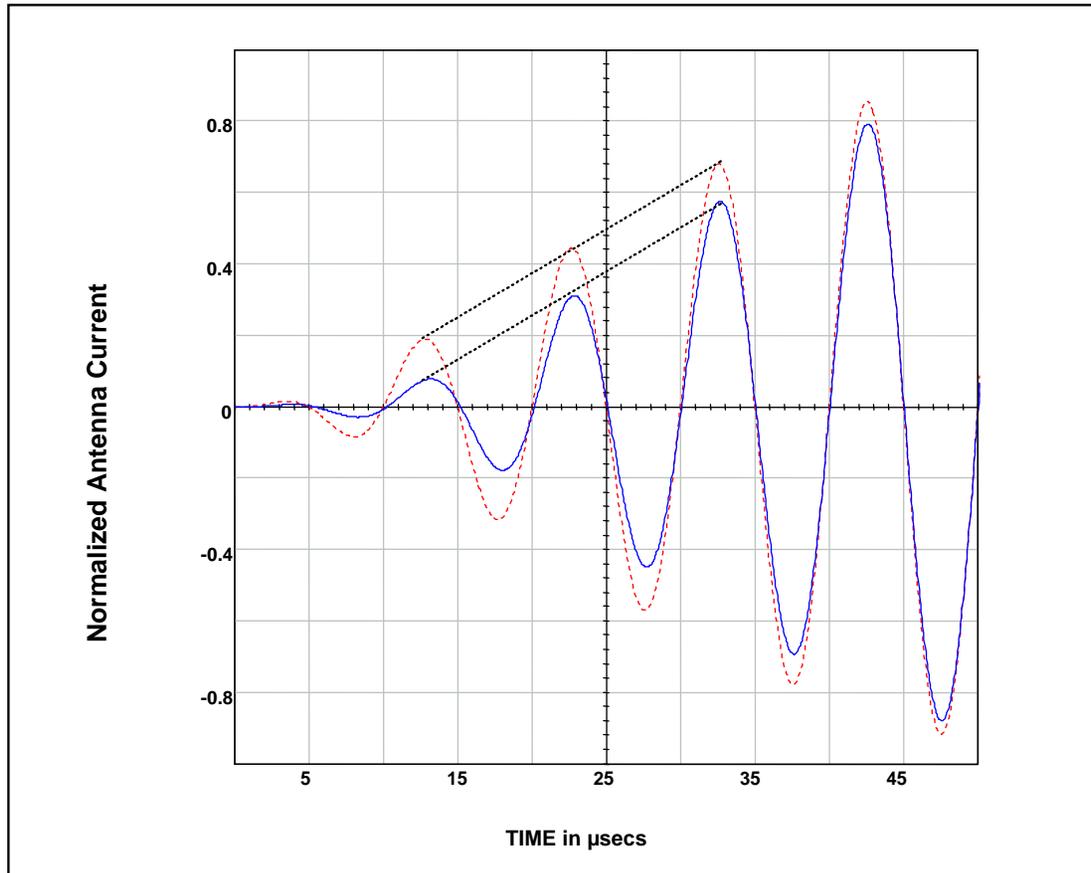


Design Verification Simulation & Tests

- Generated Loran signal spectrum



Design Verification Simulation & Tests



$$\text{ECD} = +5\mu\text{sec}$$

$$2 - 2 - 6 - 6$$

$$(2.2 - 2.1 - 6.1 - 6)$$

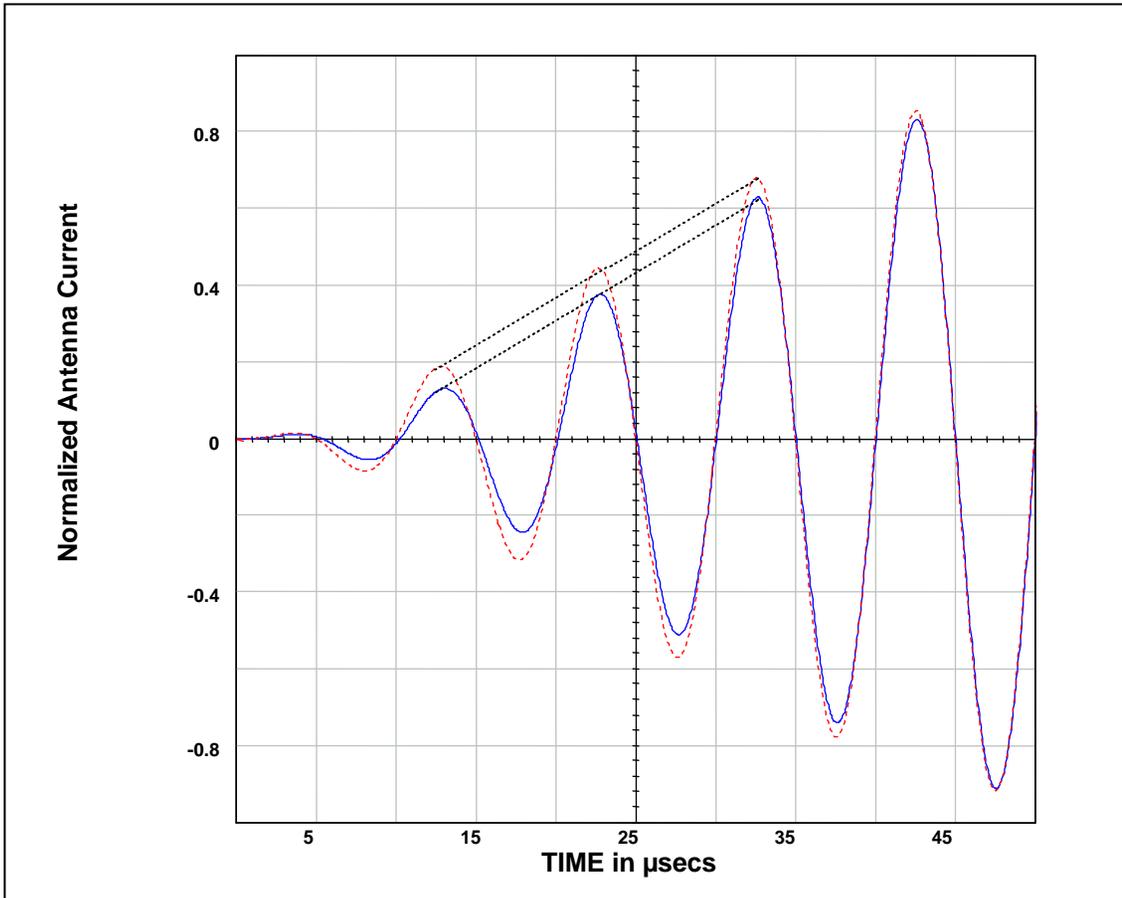
$$(E_{\text{SCR}})_{\text{MAX}} = 1650\text{v}$$

$$(E_{\text{C1}})_{\text{MAX}} = 1100\text{v}$$

$$(I_{\text{A}})_{\text{MAX}} = 665\text{A}$$



Design Verification Simulation & Tests



$$\text{ECD} = +2.5\mu\text{sec}$$

$$4 - 4 - 4 - 4$$

$$(4.2 - 4.1 - 4.03 - 4.03)$$

$$(E_{\text{SCR}})_{\text{MAX}} = 1600\text{v}$$

$$(E_{\text{C1}})_{\text{MAX}} = 1100\text{v}$$

$$(I_{\text{A}})_{\text{MAX}} = 665\text{A}$$



Design Verification Simulation & Tests

- Simulation Results

- Full range of Loran signal ECD's was generated. ECD “truth” table can be used as a reference in the design of Transmitter Control Assembly (TCA)
- The same model will be used to generate HCG reassignment table for TCA, which will be used in case of HCG failure (soft fail concept)
- Different values of Tailbiter components were analyzed with respect to tail attenuation requirements

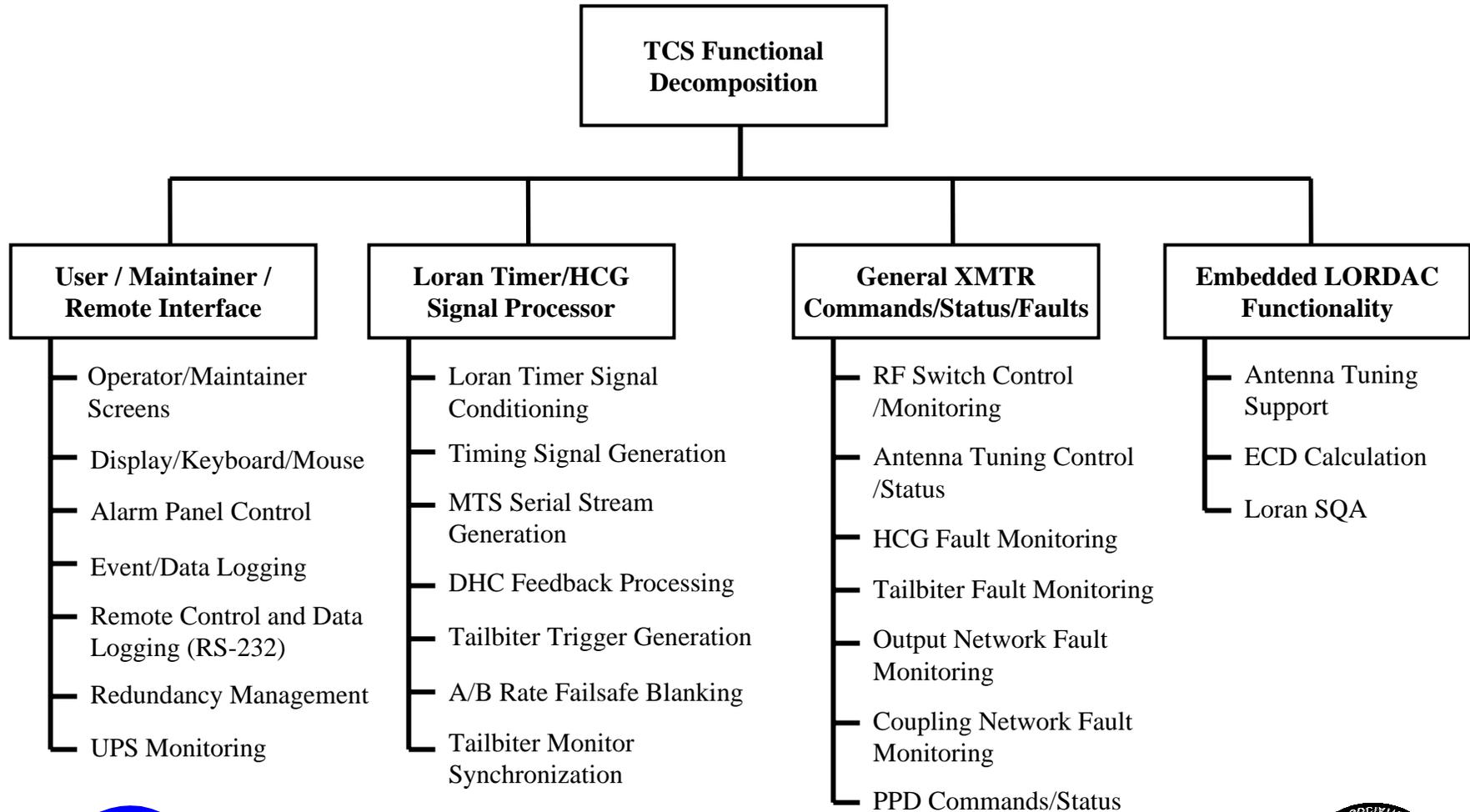


TCS Design Philosophy

- Retain Existing System Partitioning
 - GFE Loran Timer and Remote Control
 - Control Console, XMTR and Power Distribution
- Retain Existing Functionality
 - Replace TOPCO, PATCO, SDA and Display Units
 - Auto “Fail-Over”/Redundancy
- Incorporate New Functionality
 - Support for Additional Drive Half Cycles
 - Dynamic Re-Assignment of HCGs
 - Real-Time Loran Signal Quality Analysis (SQA)
 - Interpulse Modulation (Supernumerary)
- Allow for Future Capabilities
 - Intrapulse Frequency Modulation (IFM)



Functional Decomposition - Summary

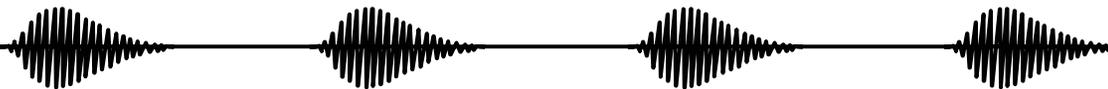
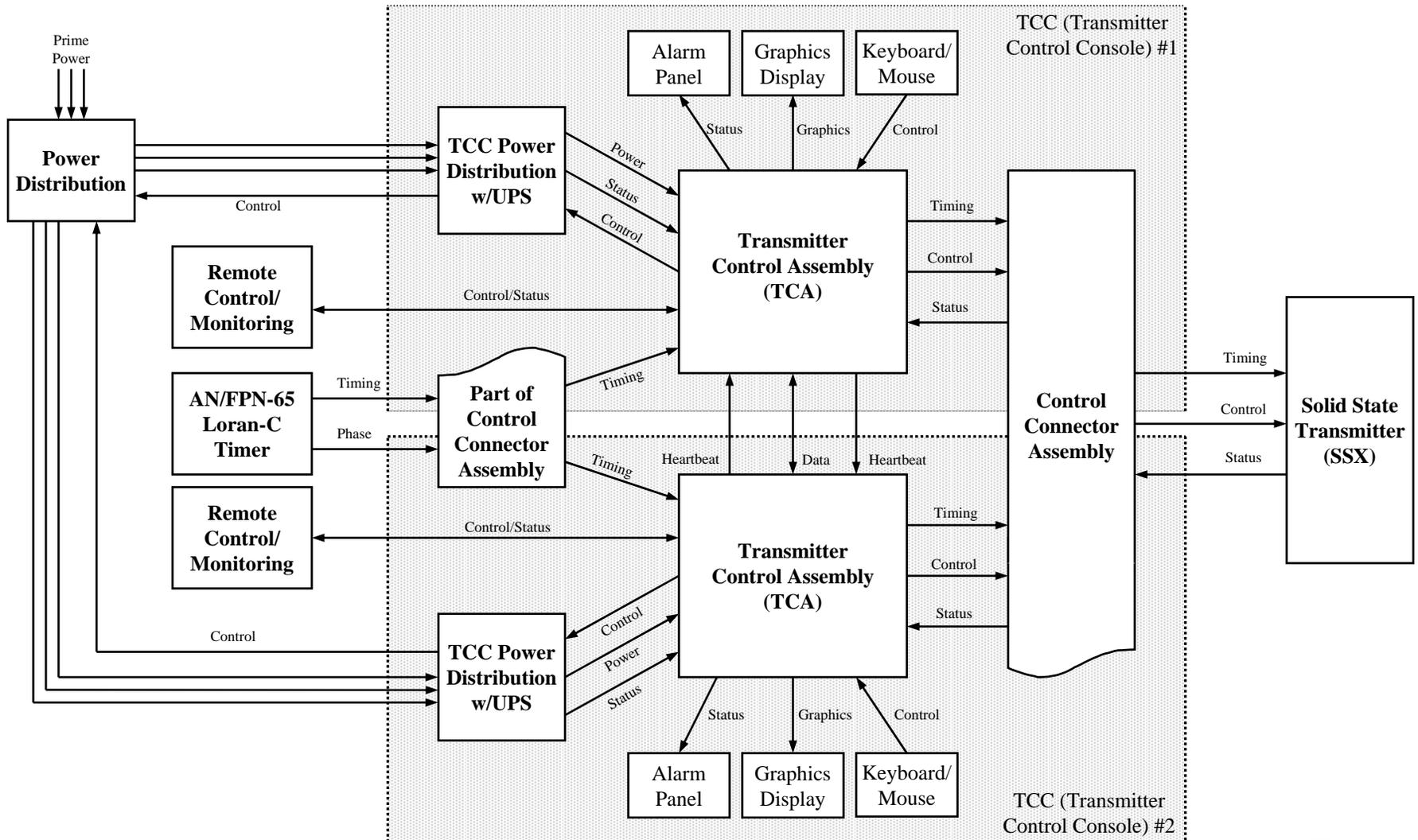


TCS Design Approach

- Redundant Design
- Commercial Off-The-Shelf (COTS) to Reduce Schedule/Technical Risk
- Card Based CPU for Reliability/Maintainability
- Hardware Independent C/C++ Software
- Graphics Display, Keyboard and Pointing Device Support
- Rear Panel Signal I/O with MS Style Connectors
- 19” Rack Mounting with Forced Air Cooling



TCS Block Diagram



Transmitter Control Subsystem

TCC (Transmitter Control Console) #1

TCC (Transmitter Control Console) #2

} *Redundant Transmitter Control Consoles*

Connector Panel Assembly

Alarm/Status Panel

Power Control

Touchscreen Display

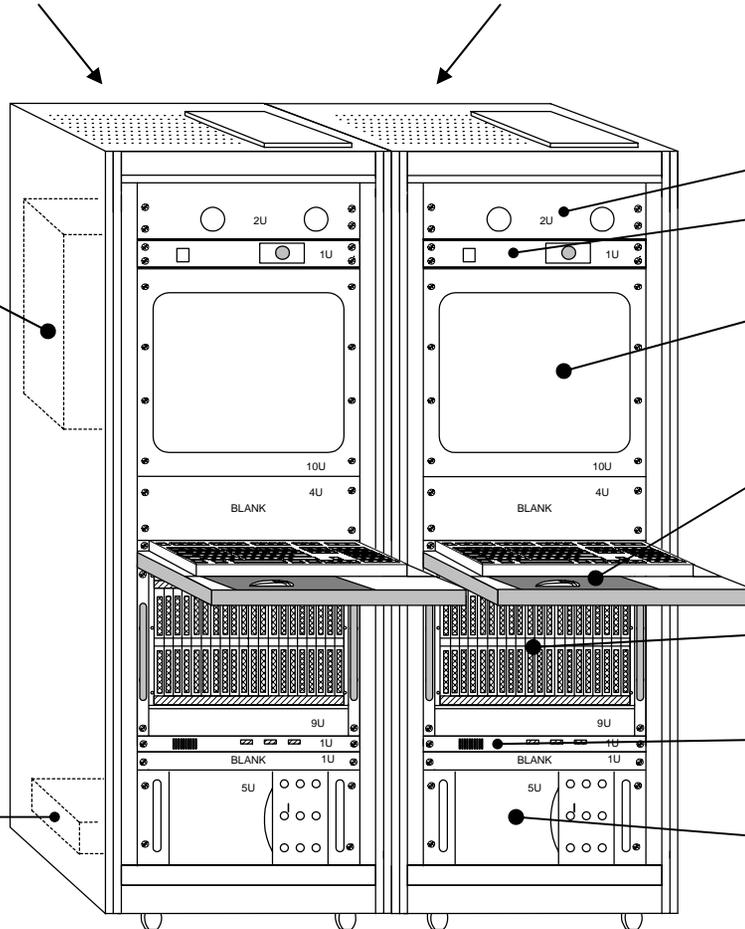
Retractable Keyboard Tray

TCA (Transmitter Control Assembly)

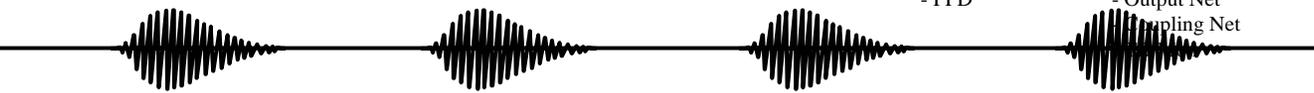
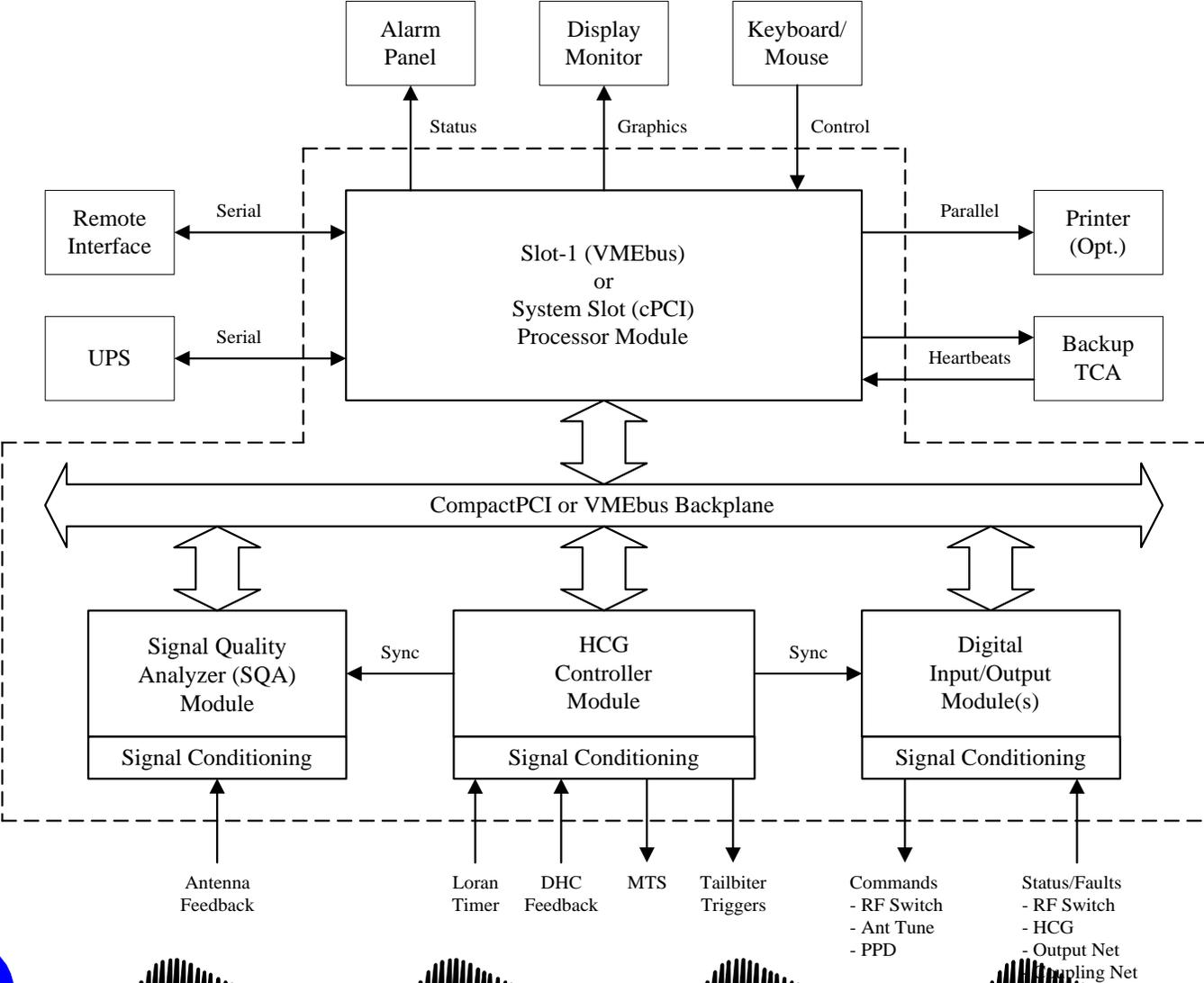
AC Input Power Phase Switcher

UPS

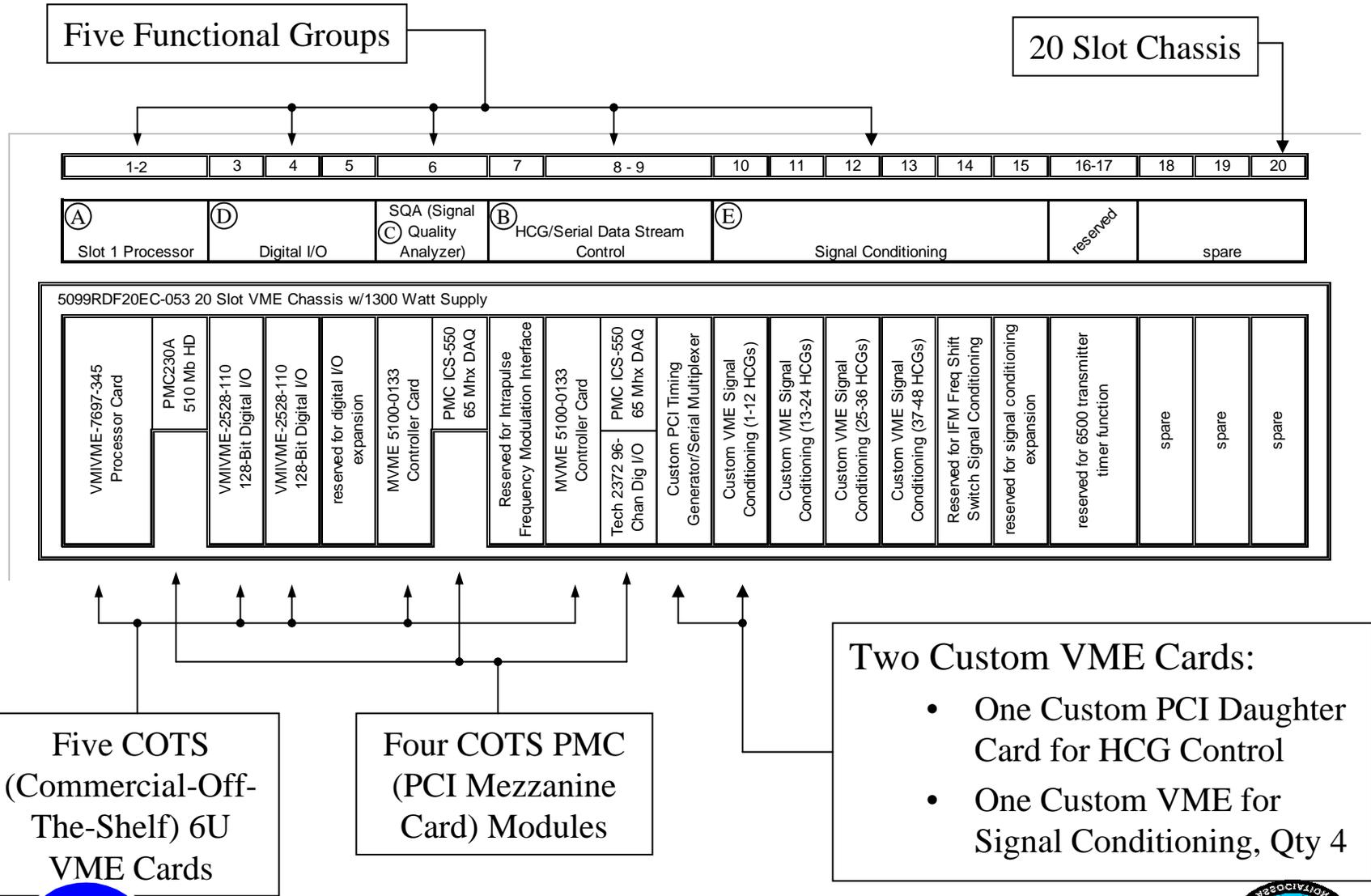
Fan Assembly



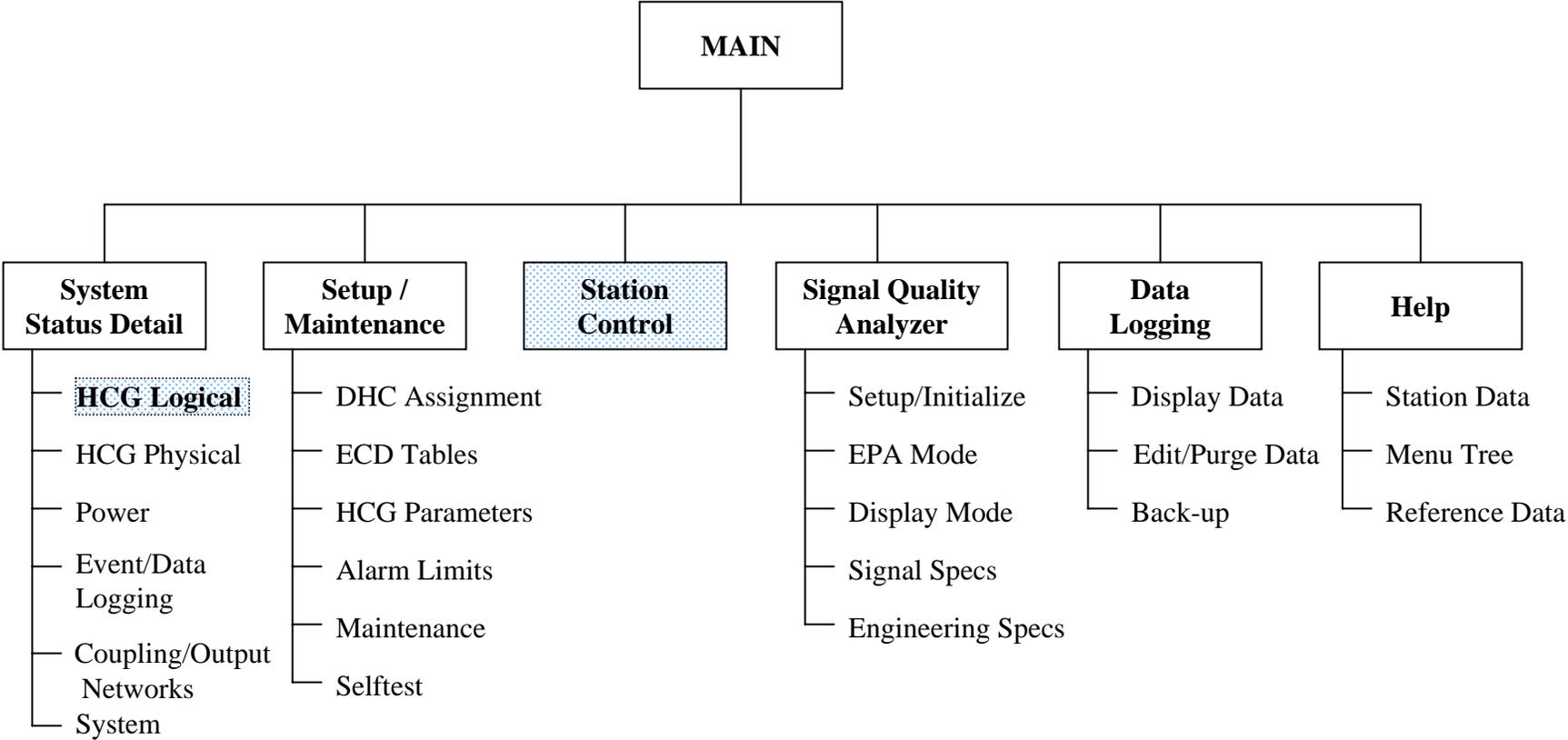
TCA Block Diagram



TCA - VME Chassis



User Interface Menu Tree



HCG Alarm/Status Screen

LORAN - C TIMING AND CONTROL ASSEMBLY

SYSTEM STATUS SUMMARY

ALARMS

HCGs OK
 POWER OK
 COUPLING NW.. OK
 OUTPUT NW..... OK
 SYSTEM..... OK

STATUS

Active Group . 1
 Transmitter ON
 Cmd ECD A ... -0.002
 Cmd ECD B ... +0.015
 GRI Rate A ... 9680
 GRI Rate B ... 8350
 DHC's 4

Positive Drive Half Cycles

Drive Cycle 1	Drive Cycle 2	OFF LINE
I 3A1,A3 _____ reset	I 3A1,A1 _____ reset	
I 3A2,A1 _____ reset	I 3A3,A1 _____ reset	
I 3A2,A3 _____ reset	II 3A1,A3 _____ reset	
I 3A3,A3 _____ reset	II 3A2,A1 _____ reset	
II 3A1,A1 _____ reset	II 3A3,A1 _____ reset	
II 3A2,A3 _____ reset	II 3A4,A1 _____ reset	
II 3A3,A3 _____ reset		
II 3A4,A3 _____ reset		

Negative Drive Half Cycles

Drive Cycle 1	Drive Cycle 2	OFF LINE
I 3A1,A4 _____ reset	I 3A1,A2 _____ reset	
I 3A2,A2 _____ reset	I 3A3,A2 _____ reset	
I 3A2,A4 _____ reset	II 3A1,A4 _____ reset	
I 3A3,A4 _____ reset	II 3A2,A2 _____ reset	
II 3A1,A2 _____ reset	II 3A3,A2 _____ reset	
II 3A2,A4 _____ reset	II 3A4,A2 _____ reset	
II 3A3,A4 _____ reset		
II 3A4,A4 _____ reset		

RESET HCG ALARMS

SILENCE HCG ALARMS

HCG
PHYSICAL

POWER

COUPLING
OUTPUT NETWORKS

SYSTEM

HCG
PHYSICAL

POWER

COUPLING
OUTPUT NETWORKS

SYSTEM

MAIN
MENU

Station Control Screen

LORAN - C TIMING AND CONTROL ASSEMBLY

SYSTEM STATUS SUMMARY

ALARMS

HCGs OK
POWER OK
COUPLING NW.. OK
OUTPUT NW..... OK
SYSTEM..... OK

STATUS

Active Group . 1
Transmitter ON
Cmd ECD A ... -0.002
Cmd ECD B ... +0.015
GRI Rate A ... 9680
GRI Rate B ... 8350

STATION CONTROL

Current Active Network	Group I	Group II	SWITCH
RF Switch	Armed	Disarmed	SWITCH
Current Primary TCA	Group I	Group II	SWITCH
Aural Alarm Status	ON	Silenced	SWITCH
Transmitter Status	ON	OFF	SWITCH
Trigger Status	Enabled	Inhibit	SWITCH

Five unlabeled rectangular buttons followed by a button labeled **MAIN MENU**.

HCG/SDSC Methodology

- HCG Control Methodology

- Current System Design Analyzed

- Similar Approach for Control of HCGs Chosen

- Reduce development

- Minimize risk

- Improve maintainability

- Timing Analyzed for Support of:

- Utilization of Additional Half Cycles to Improve Transmitter Efficiency

	1-2	3	4	5	6	7	8-9	10	11	12	13	14	15	16-17	18	19	20				
	WAVE 2004-10 PAC 200A 50 Mhz ID	PAC 200A 50 Mhz ID	WAVE 2004-10 125Mhz Signal ID	WAVE 2004-10 125Mhz Digital ID	WAVE 2004-10 125Mhz Digital ID expansion	WAVE 2004-10 Control Card	PAC CS-500 65 Mhz DMO	Reserved for Inphase Frequency Modulation (IFM) Control Card	Reserved for Inphase Frequency Modulation (IFM) Control Card	Tran 2007-06 PAC CS-600 Chan Dig IO 65 Mhz DMO	Custom PCTuning Generator/Burst Multiplexer	Custom WAVE Signal Conditioning (1-12 HCGs)	Custom WAVE Signal Conditioning (13-16 HCGs)	Custom WAVE Signal Conditioning (17-19 HCGs)	Reserved for IM Inp S/H	Switch Signal Conditioning	Reserved for Signal conditioning expansion	Reserved for 6500 transmitter Inp function	spare	spare	spare
Slot 1 Processor	Digital I/O	SQA (Signal Quality Analyzer)	HCG/Serial Data Stream Control				Signal Conditioning				Reserved	spare									

HCG Control Similar to Existing System
Control Methodology



HCG/SDSC Functions

- Main HCG/SDSC Functions are as Follows:

1-2	3	4	5	6	7	8-9	10	11	12	13	14	15	16-17	18	19	20	
WAVEFORMS Processor Card	PAC203A 50 Mbps IO	WAVE202H IO 128B/Signal IO	WAVE201H IO 128B/Signal IO	Waveform Processor ID expansion	WAVE 2000/133 Controller Card	Reserved for Impulse Frequency Modulation hardware	PAC CS-600 66 Mhz DAD Chan Dig IO	Custom I/O Timing Generator/Serial Multiplexer	Custom VME Signal Conditioning (1-16 HCGs)	Custom VME Signal Conditioning (1-16 HCGs)	Custom VME Signal Conditioning (1-16 HCGs)	Reserved for IM, PMA, SNA	Switch Signal Conditioning expansion	Reserved for 600 transceiver line function	spare	spare	spare
Slot 1 Processor	Digital I/O	SQA (Signal Quality Analyzer)	HCG/Serial Data Stream Control				Signal Conditioning				Reserved	spare					

- **Failsafe Blanking**
- **Timing and Triggering for the TCA Based on USCG Timer Signals**
- **Polarity Control for Loran Pulse Phase Coding Based on USCG Set and Reset Pulses**
- **High Speed Sampling of HCG Feedback**
 - **Adjust HCG Amplitude and Trigger Timing Based on Feedback Analysis**
- **Generate Four (4) Serial Data Streams, One for Each Group of HCGs**
- **Allocate HCGs to Required Drive Cycle Based on Programmed System Settings**
- **Generate Transmitter Tailbiter Triggers**
- **Future Generation of FSS (Frequency Shift Switches) Control Signals for IFM Based on Coast Guard Control**



HCG/Serial Controller Software

- Functions Performed
 - Initializes MTS Data, Tailbiter Trigger and Frequency Shift Switch Control Signal Data Buffers
 - Monitors DHC Feedback Signal from DAQ HW Module
 - Computes DHC Magnitude and Zero Crossing Values
 - Based on These Computed Values, Adjusts MTS Amplitude and Delay Values as Required
 - Loops Once per LORAN Pulse
 - Provides All Data for Use by Main Processor
 - Performs Self Health Monitoring
 - Inhibits Signal Outputs if in Backup Mode



Signal Quality Analyzer (SQA) Group

- The SQA Group Consists of the Following:

1-2		3	4	5	6	7	8-9		10	11	12	13	14	15	16-17	18	19	20		
VMVME-7697-345 Processor Card		PMC230A 510 Mb HD	VMVME-2628-110 128-Bit Digital I/O	VMVME-2628-110 128-Bit Digital I/O reserved for digital I/O expansion	VMVME 5100-0133 Controller Card	PMC ICS-550 65 Mhz DAQ	Reserved for Intrapulse Frequency Modulation Interface		VMVME 5100-0133 Controller Card	Tech 2372 96- Chan Dig I/O 65 Mhz DAQ	Custom PCI Timing Generator/Serial Multiplexer	Custom VME Signal Conditioning (1-12 HCGs)	Custom VME Signal Conditioning (15-24 HCGs)	Custom VME Signal Conditioning (25-36 HCGs)	Custom VME Signal Conditioning (37-48 HCGs)	Reserved for IFM/Freq Shift Switch Signal Conditioning reserved for signal conditioning expansion	reserved for 6500 transmitter timer function	spare	spare	spare
Slot 1 Processor		Digital I/O			SQA (Signal Quality Analyzer)	HCG/Serial Data Stream Control		Signal Conditioning			reserved		spare							

- One (1) Processor Card [MVME5100-013]
 - One (1) 65 Mhz DAQ (Data Acquisition) PMC Card [ICS-550]
- Main SQA Functions are as follows:
 - High Speed Sampling of Antenna Feedback
 - Adjust Antenna Tuning Based on Feedback Analysis
 - The Functional Capability of the PC-LORDAC Test capability includes both Signal Specification tests and Engineering Specification tests
 - Future Analysis of Output Waveform for Intrapulse Frequency Modulation



Summary

- Cost Effective
- Higher Efficiency
- Managed Risk
- Flexible Control Architecture
- Familiar Assemblies
- Enhanced Maintainability and Operability

