

IGBT Gate Drive Considerations

Introduction

The IGBT transistor is a much more complex structure than either a MOSFET or a Bipolar Junction Transistor (BJT). It combines features of both of these devices and has three terminals – a gate, a collector and an emitter. In terms of the gate drive, the device behaves like a MOSFET. The current carrying path is very similar to the collector–emitter path of a BJT. Figure 1 shows the equivalent device circuit for an n type IGBT.

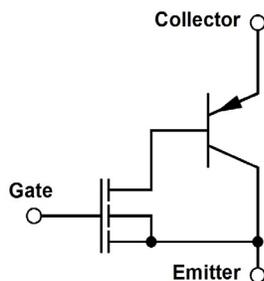


Figure 1. Equivalent Circuit

Basic Drive Understanding

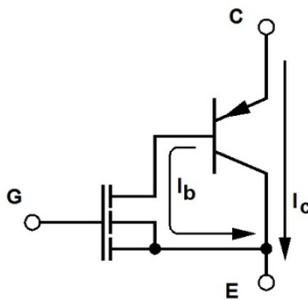


Figure 2. Turn on Current Flow

To turn a BJT on and off quickly, the gate current must be driven hard in each direction to move the carriers into and out of the base region. When the gate of the MOSFET is driven high, there is a low impedance path out of the base of the bipolar transistor to its emitter. This turns that transistor on quickly, so the faster the gate is driven high, the faster the collector current begins to flow. The base and collector current flows are shown in Figure 2.



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APPLICATION NOTE

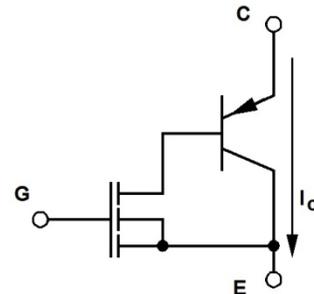


Figure 3. Turn off Current Flow

The turn off scenario is a bit different and is shown in Figure 3. When the gate of the MOSFET is pulled low, there is no current path for the base current in the BJT. The lack of base current begins the turn off process; however, for a fast turn off, current should be forced into the base terminal. There is no mechanism available to sweep the carriers out of the base, so the turn off of the BJT is relatively slow. This leads to a phenomenon called tail current since the stored charge in the base region must be swept away by the emitter current.

It should be obvious that faster gate drive dv/dt rates (due to higher gate current capability) will turn the IGBT on and off faster, but there are inherent limitations as to how fast the device can switch, especially for turn off. Due to these limitations switching frequencies are often in the 20 kHz to 50 kHz range, although in special cases they can be used in faster and slower circuits. IGBTs are generally used in high power ($P_o > 1$ kW) circuits in both resonant and hard-switching topologies. Resonant topologies minimize the switching losses as they are either zero voltage switching or zero current switching.

Slower dv/dt rates offer improved EMI performance, when that is of concern and cause less spiking during the turn-on and turn-off transitions. This is at the expense of lower efficiency due to the slower turn on and turn off times.

Secondary Turn-on

There is a phenomenon that occurs with MOSFETs called secondary turn on. It is due to the very fast dv/dt rates on the drain voltage which can be in the range of 1000 – 10,000

V/us. Though IGBTs don't typically switch as fast as a MOSFET they can still experience very high dv/dt levels due to the high voltages used. This can lead to secondary turn on if the gate resistance is too high.

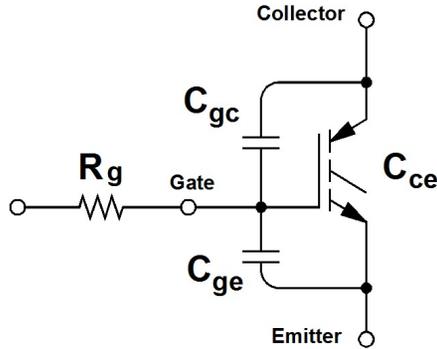


Figure 4. IGBT with Parasitic Capacitances

Under this condition, when the gate is being pulled low by the driver the device begins to turn off, but the rise in voltage on the collector generates a voltage on the gate due to the voltage divider of Cgc and Cge. If the gate resistor is too high, the gate voltage can climb high enough to turn the device back on. This causes a large pulse of power which can overheat, and in some cases destroy the device.

The limiting equation for this problem is:

$$\frac{dv}{dt} < \frac{V_{th}}{R_g \cdot C_{gc}} \quad [\text{Ref. 1}] \quad (\text{eq. 1})$$

Where:

- dv/dt is the rate of the rising voltage waveform on the collector at turn off
- V_{th} is the plateau level of the gate
- R_g is the total gate resistance
- C_{gc} is the gate–emitter capacitance

It should be noted that C_{iss} on the data sheet is the parallel equivalent of the Cge and Cgc capacitances.

Similarly, R_g is the series sum of the gate driver impedance, the physical gate resistor and the internal gate resistance. The internal gate resistance may be given on the data sheet. If not, it can be measured by using an LCR bridge and shorting the collector–emitter pins and then measuring the equivalent, series RC at a frequency close to the switching frequency.

The driver impedance may be found on its data sheet if it uses a FET output stage. If it is not on the data sheet, it can be approximated by taking the peak drive current at its rated V_{CC} level.

$$R_{\text{driver}} \cong \frac{V_{CC}}{I_{pk}} \quad (\text{eq. 2})$$

So the maximum total gate resistance is:

$$R_g < \frac{V_{th}}{C_{gc} \cdot \left(\frac{dv}{dt}\right)} \quad (\text{eq. 3})$$

The maximum dv/dt is based on the gate drive current as well as the circuit impedances surrounding the IGBT and needs to be verified in the actual circuit if a high value resistor is used for the gate drive. Figure 5 shows turn off waveforms for three different IGBTs in the same motor control circuit. The dv/dt is 3500 V/μs in this application.

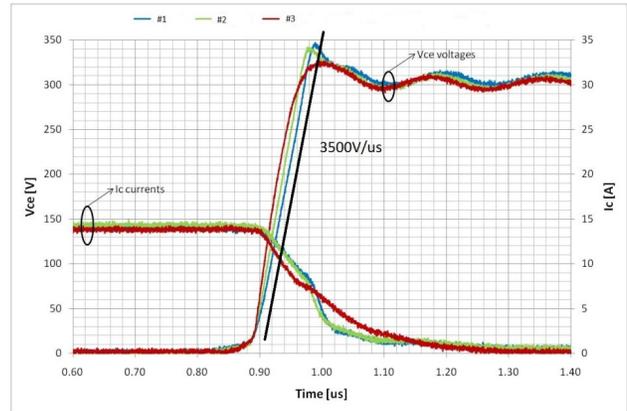


Figure 5. Turn Off Waveforms for 3 IGBTs

For this situation, IGBT #2 has a typical C_{gc} of 84 pF and a threshold gate voltage (at 15 A) of 7.5 V.

Using the above equation, the maximum total gate resistance for this circuit would be:

$$R_g < \frac{7.5 \text{ V}}{84 \text{ pF} \cdot \left(\frac{3500 \text{ V}}{\mu\text{s}}\right)} \quad (\text{eq. 4})$$

R_g < 25.5 Ω

So if the internal gate resistance is 2 Ω and the driver impedance is 5 Ω, the absolute largest gate resistor should be 18 Ω. In practice, due to variations in IGBTs, drivers, board impedances and temperature, a maximum value of something lesser (e.g. 12 Ω) would be advisable.

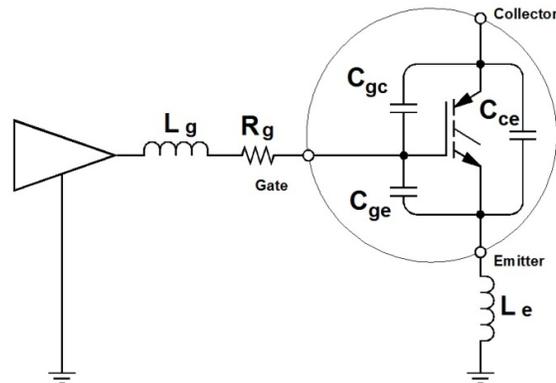


Figure 6. Equivalent Gate Drive Circuit

Gate Ringing

It may appear that eliminating an external gate resistor would give optimum high frequency performance, while assuring that secondary turn on would not occur. In some cases this may work, but it can also lead to oscillations due to the impedances in the gate drive circuit.

The gate drive circuit is a series RLC tank circuit. The capacitance comes mainly from the IGBT parasitic capacitances. The two inductances shown, come from a combination of the board trace inductance and the bond wire inductance of the IGBT and driver.

With little or no gate resistance, the tank circuit will oscillate and cause high losses in the IGBT. Enough gate resistance is required to dampen the tank circuit and therefore eliminate oscillations.

It is difficult to calculate the proper resistor as the inductance is difficult to measure. Good layout procedures are the best solution to minimizing the required, minimum gate resistance.

The path between the driver and IGBT gate should be as short as possible. This means the entire circuit path of the gate drive as well as the ground return path. If the controller does not include an integrated driver, it is much more important to locate the IGBT driver close to the gate of the

IGBT than it is to locate the input of the gate driver to the PWM output of the controller. The current from the controller to the driver is very small and any stray capacitance will have much less of an effect than with the high currents and di/dt levels from the driver to the IGBT. Short, wide traces are the best way to minimize the inductance.

Typical minimum driver resistances range from 2 Ω to 5 Ω. This includes the driver impedance, external resistor value and internal IGBT gate resistance value.

Once the board is laid out, the gate resistor value can be determined and optimized.

Conclusion

Guidelines have been given for the minimum and maximum values of the gate resistor values. There is a range of values between these limits that will allow tuning of the circuit for maximum efficiency, minimum EMI or other important parameters. Designing a circuit with values safely between these extremes will offer a robust design.

References:

1. *Power Semiconductor Devices*, B. Jayant Baliga, PWS publishing Company, Boston. ISBN 0-534-94098-6

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